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05/30/00

Express Mail #EL010285829US

Asst. Commissioner for Patents

Washington, DC 20231

OFGS File No. :P/1071-993  
Inventor :Teruhisa Tsuru et al.  
Title :DELAY LINE  
Assignee :Murata Manufacturing Co., Ltd.

Enclosed herewith please find the following documents in the above-identified application for United States Letters Patent:

- 14 Pages of Specification including Abstract and Claims  
15 Numbered Claims Calculated as 15 Claims for Fee Purposes  
7 Sheets of Drawing Containing Figures 1A to 9. (Informal)  
X Declaration and Power of Attorney  
X Priority is Claimed under 35 U.S.C. §119:  
Convention Date June 1, 1999 for Japan Appln. S.N. 11-154044  
X Certified Priority Application  
       Verified Statement Claiming Small Entity Status under 37 C.F.R. §1.27.  
X Assignment  
X Return-Addressed Post Card

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- 1 -

DELAY LINEBACKGROUND OF THE INVENTION

## 1. Field of the Invention

5 The present invention relates to delay lines used for delaying signal transmission in computers, measurement apparatuses, and the like. More specifically, the invention relates to delay lines in which delay time can be adjusted.

## 2. Description of the Related Art

10 Fig. 9 is a top view of a prior art example of a delay line. A delay line 80 has a structure in which a transmission line 82 used for a signal line is folded in a meandering manner and disposed on one of the main surfaces of a dielectric substrate 81, and a ground conductor (not shown) is disposed on substantially all of the other main surface of the dielectric substrate 81. The ends of the transmission line 82 are connected to an input terminal 83, and an output terminal 84, respectively. The entire length of the transmission line 82 determines the delay time between the input terminal 83 and the output terminal 84. In order to change the delay time, as shown in Fig. 9, an intermediate tap terminal 85 is disposed at a certain point on the meandering transmission line 82 and used, for example, as an output terminal, thereby providing a different delay time. The intermediate tap terminal 85 is adapted to be connected to the transmission line 82 at different positions, whereby the delay time can be changed by changing the position.

20 However, in the case of the above delay line, when the position of an output terminal has been set according to a desired delay time, it is impossible to adjust the delay time again, after the delay line has been mounted in a printed circuit board or the like.

25 In addition, since one of the three terminals is not used, the unused terminal

generates a capacitance or works as a stub, which leads to a problem of causing the reflection of a signal.

In addition, as shown in Fig. 9, when a transmission line to be used has a meandering configuration, an intermediate tap terminal can be connected only to the lower-side curved part of the meandering transmission line. As a result, it is impossible to adjust delay time continuously.

### SUMMARY OF THE INVENTION

To overcome the above described problems, embodiments of the present invention provide a delay line in which delay time can be adjusted even after being mounted on a printed circuit board, and in which the delay time can continuously be adjusted.

One preferred embodiment of the present invention provides a delay line comprising: a dielectric substrate including a pair of main surfaces; a transmission line disposed on one of the main surfaces of the dielectric substrate; a ground conductor disposed on the other of the main surfaces of the dielectric substrate; and a capacitance, provided by at least one of a variable capacitor and a diode, for example, being disposed on the dielectric substrate and connected to the transmission line, advantageously in parallel with the transmission.

According to the above described structure and arrangement, by changing the capacitance of the variable capacitor or the diode, a frequency of an attenuation pole in the pass characteristic of the delay line can be continuously changed even after the delay line is mounted on a printed circuit board. As a result, the delay time of the delay line can be continuously changed so as to obtain a desired delay time.

Another embodiment of the present invention provides a delay line comprising: a multilayer structure formed by laminating a plurality of dielectric layers; a transmission line embedded in the multilayer structure; a plurality of ground conductors disposed on the dielectric layers and being separated from each other by

the transmission line and the dielectric layer; and at least one of a variable capacitor and a diode being disposed on the multilayer structure and connected in parallel to the transmission line.

5 According to the above described structure and arrangement, in addition to the advantages of the first embodiment, the transmission line is formed inside the multilayer structure in which the plurality of the dielectric layers are laminated. Therefore, the wiring between the transmission line and the variable capacitor can also be formed inside the multilayer structure. Therefore, losses caused by the wiring can be suppressed, and it is possible to obtain a delay line having more  
10 satisfactory characteristics.

Other features and advantages of the present invention will become apparent from the following description of embodiments of the invention which refers to the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

15 Fig. 1A shows a top view of a delay line according to a first embodiment of the present invention, and Fig. 1B shows a sectional view thereof.

Fig. 2 shows an equivalent circuit diagram of the delay line shown in Figs. 1A and 1B.

20 Fig. 3 shows a graph illustrating the pass characteristics of the delay line shown in Figs. 1A and 1B, and the frequency dependence of the delay time of the delay line.

Fig. 4 shows a graph illustrating the capacitance dependence of the delay time of the delay line shown in Figs. 1A and 1B.

25 Fig. 5 is an exploded perspective view of a delay line according to a second embodiment of the present invention.

Fig. 6 is a sectional view of a modified example of the delay line shown in Fig. 5.

Fig. 7 is an exploded perspective view of a delay line according to a third embodiment of the present invention.

Fig. 8 is a graph illustrating an applied voltage dependence of the delay time of the delay line shown in Fig. 7.

5 Fig. 9 is a top view illustrating a prior art delay line.

#### DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Fig. 1A shows a top view of a delay line according to a first embodiment of the present invention, and Fig. 1B shows a sectional view thereof. A delay line 10 has a dielectric substrate 11. A transmission line 12 used for a signal line is disposed on one of the main surfaces of the dielectric substrate 11. The transmission line 12 is folded in a meandering manner. On substantially the entire back surface of the dielectric substrate 11, a ground conductor 13 is formed.

A variable capacitance trimmer capacitor 14 is connected in parallel to the transmission line 12. In addition, the ends of the transmission line 12 are connected to an input terminal 15 and an output terminal 16, respectively. The ground conductor 13 is connected to ground terminals 17 and 18, respectively.

Fig. 2 is an equivalent circuit diagram of the delay line shown in Fig. 1. The delay line 10 has a structure in which an inductance component  $L$  of a micro strip line formed by the transmission line 12 and the ground conductor 13 are connected in parallel to a capacitance  $C$  of the trimmer capacitor 14 between the input terminal 15 and the output terminal 16.

In addition, in the pass characteristics, an attenuation pole is generated at a frequency obtained by an expression  $1/(2\pi (L \cdot C)^{1/2})$ . With the attenuation pole, phase changes occur in high frequency signals passing through the transmission line 12. As a result, the delay time of the delay line 10 changes according to frequency.

Fig. 3 shows a graph illustrating the pass characteristic of the delay line 10 shown in Fig. 1, and the frequency dependence of delay time thereof. In this figure,

a solid line P indicates the pass characteristic, and a broken line D indicates the delay time. The inductance component L of the transmission line 12 is 20 (nH), and the capacitance C of the trimmer capacitor 14 is 0.5 (pF).

5 This figure shows that, in the pass characteristics, an attenuation pole occurs near a frequency of 1.6 (GHz) obtained by the expression  $1/(2\pi \sqrt{L \cdot C})$ , and due to the influence of the attenuation pole, the delay time greatly changes.

10 Fig. 4 is a graph illustrating the capacitance dependence of the delay time of the delay line 10 shown in Fig. 1. In Fig. 4, the horizontal axis of the graph indicates the capacitance of the trimmer capacitor 14, and the vertical axis thereof indicates the delay time of the delay line 10. In addition, a solid line D1 shows changes of the delay time at a frequency of 1.5 GHz, and a broken line D2 shows changes of the delay time at a frequency of 1.7 GHz.

15 This figure shows that adjustment of the capacitance of the trimmer capacitor 14 permits the delay time of the delay line 10 to be adjusted. The reason for this is that when the capacitance of the trimmer capacitor 14 is changed, the frequency of the attenuation pole, which is obtained by the expression  $1/(2\pi \sqrt{L \cdot C})$ , also changes.

20 In the delay line of the first embodiment described above, since the variable trimmer capacitor is connected in parallel to the transmission line, continuously changing the capacitance of the trimmer capacitor also continuously changes the frequency at which the attenuation pole occurs in the pass characteristic. As a result, it is possible to continuously change the delay time of the delay line so as to obtain a desired delay time.

25 Fig. 5 is an exploded perspective view of a delay line according to a second embodiment of the present invention. A delay line 20 has a rectangular-parallelepiped multilayer structure 21 obtained by sequentially laminating rectangular dielectric layers 211 to 215 formed of dielectric ceramic materials (relative permittivity  $\epsilon_r$  : approximately 6.0), whose main components comprise

barium oxide, aluminum oxide, and silica, bonding by pressurizing and then integrally firing at temperatures of 800 to 1000° C. On the side surfaces and upper and lower surfaces of the multilayer structure 21, an input terminal 22, an output terminal 23, and two ground terminals 24 and 25 are formed.

5           Substantially rectangular ground conductors 261 and 262 are formed on the upper surfaces of the dielectric layers 211 and 213, respectively. In addition, a transmission line 27 is disposed on the upper surface of the dielectric layer 212 in a substantially meandering form. Furthermore, substantially rectangular capacitor electrodes 281 and 282 are formed on the upper surfaces of the dielectric layers 214 and 215, respectively.

10           In this case, both ends of the transmission line 27 formed on the upper surface of the dielectric layer 212, and parts of the ground conductors 261 and 262 formed on the upper surfaces of the dielectric layers 211 and 213 are extended onto the side surfaces of the multilayer structure 21 to be connected to the input terminal 22, the output terminal 23, and the ground terminals 24 and 25, respectively.

15           In addition, an end of the transmission line 27 on the upper surface of the dielectric layer 212 is connected to the capacitor electrode 281 on the upper surface of the dielectric layer 214 by a via-hole conductor 291 disposed in such a manner that the via-hole conductor 291 passes through the dielectric layers 213 and 214.

20           Furthermore, the other end of the transmission line 27 on the upper surface of the dielectric layer 212 is connected to the capacitor electrode 282 on the upper surface of the dielectric layer 215 by a via-hole conductor 292 disposed in such a manner that the via-hole conductor 291 passes through the dielectric layers 213 to 215.

25           With such a structure, in the delay line 20, between the input terminal 22 and the output terminal 23, the inductance component L of the strip line formed by the transmission line 27 and the ground conductors 261 and 262 is connected in parallel to the capacitance component C of the variable capacitor 28 formed by the capacitor

electrodes 281 and 282.

In this case, the equivalent circuit of the delay line 20 is the same as the equivalent circuit of the delay line 10 shown in Fig. 2.

5 The input terminal 22, the output terminal 23, and the ground terminals 24 and 25 are formed by firing printed conductive paste simultaneously with the multilayer structure 21, or by baking the printed conductive paste after the multilayer structure 21 has been fired.

10 After this, the capacitor electrode 282 formed on the upper surface of the multilayer structure 21 is trimmed by a laser or the like, by which the capacitance of the variable capacitor 28 can be continuously changed to set the delay time of the delay line 20, as in the delay line 10 (Fig. 1) of the first embodiment.

15 Fig. 6 is a sectional view of a modified example of the delay line shown in Fig. 5. When compared with the delay line 20 shown in Fig. 5, the structure of the delay line 20a is different in that it includes a trimmer capacitor 28a, as an alternative to the variable capacitor 28 (Fig. 5) formed by the capacitor electrodes 281 and 282, on the upper surface of the multilayer structure 21a having ground conductors 261a and 262a, and a transmission line 27a formed therein.

20 In this case, the transmission line 27a is connected to the trimmer capacitor 28a by via-hole conductors 291a and 292a disposed inside the multilayer structure 21a.

25 In the delay line of the second embodiment described above, since the capacitance of the trimmer capacitor can be continuously changed, even after being mounted on a printed circuit board, a frequency at which an attenuation pole occurs in the pass characteristics can also be continuously changed. As a result, the delay time of the delay line can be continuously changed so as to obtain a desired delay time.

In addition, since the transmission line is formed inside the multilayer structure in which the plurality of the dielectric layers are laminated, the wiring

between the transmission line and the variable capacitor can be formed inside the multilayer structure. As a result, losses caused by the wiring can be suppressed, and a delay line having more satisfactory characteristics can thereby be obtained.

Fig. 7 is an exploded perspective view of a delay line according to a third embodiment of the present invention. A delay line 30 has a rectangular-parallelepiped multilayer structure 31 obtained by sequentially laminating rectangular dielectric layers 311 to 314 formed of dielectric ceramic materials (relative permittivity  $\epsilon_r$  : approximately 6.0), whose main components comprise barium oxide, aluminum oxide, and silica, bonding by pressurizing, and then integrally firing at temperatures of 800 to 1000° C.

A varicap diode 32 is mounted on the upper surface of the multilayer structure 31. An input terminal 33, an output terminal 34, and two ground terminals 35 and 36 are formed on the side surfaces of the multilayer structure 31, and the upper and lower surfaces thereof.

Substantially rectangular ground conductors 371 and 372 are formed on the upper surfaces of the dielectric layers 311 and 313. In addition, a transmission line 38 having a substantially meandering configuration is formed on the upper surface of the dielectric layer 312.

In this case, both ends of the transmission line 38 formed on the dielectric layer 312, and parts of the ground conductors 371 and 372 formed on the upper surfaces of the dielectric layers 311 and 313 are extended onto the side surfaces of the multilayer structure 31 to be connected to the input terminal 33, the output terminal 34, and the ground terminals 35 and 36, respectively.

In addition, an end of the transmission line 38 on the upper surface of the dielectric layer 312 is connected to an end of the varicap diode 32 mounted on the multilayer structure 31 by a via-hole conductor 391 disposed in such a manner that the via-hole conductor 391 passes through the dielectric layers 313 and 314.

Furthermore, the other end of the transmission line 38 on the upper surface of

the dielectric layer 312 is connected to the other end of the varicap diode 32 mounted on the multilayer structure 31 by a via-hole conductor 392 disposed in such a manner that the via-hole conductor 392 passes through the dielectric layers 313 and 314.

5 With such an arrangement, in the delay line 30, between the input terminal 33 and the output terminal 34, the inductance component L of the strip line formed by the transmission line 38 and the ground conductors 371 and 372 are connected in parallel to the capacitance component C of the varicap diode 32.

In this case, the equivalent circuit of the delay line 30 is the same as the equivalent circuit of the delay line 10 shown in Fig. 2.

10 As in the case of the delay line 20 of the second embodiment, the input terminal 33, the output terminal 34, and the ground terminals 35 and 36 are formed either by firing printed conductive paste simultaneously with the multilayer structure 31, or by baking the printed conductive paste after the multilayer structure 31 is fired.

15 With this structure by changing the voltage applied to the varicap diode 32 mounted on the upper surface of the multilayer structure 31, the capacitance component of the varicap diode 32 can also be changed continuously. As a result, the delay time of the delay line 30 can be continuously changed, as in the cases of the delay lines 10 (Fig. 1) and 20 (Fig. 5) of the first and second embodiments.

20 Fig. 8 is a graph showing changes of the delay time of the delay line shown in Fig. 7. In Fig. 8, the horizontal axis of the graph indicates a voltage applied to the diode 32, and the vertical axis thereof indicates the delay time of the delay line. A solid line D3 shows changes of the delay time at a frequency of 1.5 GHz, and a broken line D4 shows changes of the delay time at a frequency of 1.7 GHz.

25 This graph shows that, when the voltage applied to the varicap diode 32 is changed, the delay time of the transmission line 38 can be changed. The reason for this is that changing the voltage applied to the varicap diode 32 changes the capacitance component of the varicap diode 32, by which a frequency at which the

attenuation pole occurs in the pass characteristics is also changed, since the varicap diode is connected in parallel to the transmission line.

In the first to third embodiments, the dielectric layers have been formed of ceramic materials whose main components comprise barium oxide, aluminum oxide, and silica. However, any material can be used as long as the value of the relative permittivity ( $\epsilon_r$ ) is 1 or greater. For example, a ceramic material whose components comprise magnesium oxide and silica or a material of fluoropolymers can be used to obtain the same advantages.

In addition, a description has been given of cases in which either a variable capacitor or a diode is connected to the transmission line. Alternatively, both a variable capacitor and a diode may be connected to the transmission line, advantageously in parallel thereto.

Although the first embodiment has described the use of a variable capacitor connected in parallel to the transmission line, the same advantages can also be obtained by using a diode on the dielectric substrate.

In the second and third embodiments, the ground conductors are disposed inside the multilayer structure. However, any way of arranging the ground conductors can be applied as long as the dielectric layer is disposed between the transmission line and the ground conductors. Alternatively, the ground conductors may be disposed on outer surfaces of the multilayer structure.

In addition, in the above description, via-hole conductors are used for connecting the transmission line to the variable-capacity capacitor and the diode, respectively. Alternatively, the same advantages can also be obtained by using through-hole conductors.

Further, although all of the disclosed embodiments have the equivalent circuit shown in Fig. 3, other circuit arrangements may be used as long as a variable capacitance is connected to a transmission line so as to be able to continuously adjust a desired delay time of the delay line.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit of the invention.

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WHAT IS CLAIMED IS:

1. A delay line comprising:  
a dielectric substrate including a pair of main surfaces;  
a transmission line disposed on one of the main surfaces of the dielectric  
substrate;  
a ground conductor disposed on the other of the main surfaces of the  
dielectric substrate; and  
a capacitance being disposed on the dielectric substrate and connected to the  
transmission line for setting a desired delay time of the delay line.
2. A delay line according to claim 1, wherein said capacitance is adjustable.
3. A delay line according to claim 2, wherein said capacitance is provided by  
a variable capacitor.
4. A delay line according to claim 2, wherein said capacitance is provided by  
a varicap diode.
5. A delay line according to claim 1, wherein said capacitance is provided by  
a diode.
6. A delay line according to claim 5, wherein said diode is a varicap diode.
7. A delay line according to claim 1, wherein said capacitance is connected  
in parallel to the transmission line.
8. A delay line comprising:  
a multilayer structure formed by laminating a plurality of dielectric layers;

a transmission line formed on a dielectric layer embedded in the multilayer structure;

- 5 a plurality of ground conductors disposed on the dielectric layers and a pair of said ground conductors being disposed on opposite sides of the transmission line; and

a capacitance disposed on the multilayer structure and connected to the transmission line for setting a desired delay time of the delay line.

9. A delay line according to claim 8, wherein said capacitance is adjustable.

10. A delay line according to claim 9, wherein said capacitance is provided by electrodes formed on respective ones of said dielectric layers.

11. A delay line according to claim 9, wherein said capacitance is provided by a variable capacitor.

12. A delay line according to claim 9, wherein said capacitance is provided by a varicap diode.

13. A delay line according to claim 8, wherein said capacitance is provided by a diode.

14. A delay line according to claim 13, wherein said diode is a varicap diode.

15. A delay line according to claim 8, wherein said capacitance is connected in parallel to the transmission line.

DELAY LINEABSTRACT OF THE DISCLOSURE

5 A delay line comprising a dielectric substrate including a pair of main  
surfaces; a transmission line disposed on one of the main surfaces of the dielectric  
substrate; a ground conductor disposed on the other of the main surfaces of the  
dielectric substrate; and at least one of a variable capacitor and a diode being  
disposed on the dielectric substrate and connected in parallel to the transmission line  
for setting a desired delay time of the delay line. In the above delay line, the delay  
10 time can be adjusted even after the delay line is mounted on a printed circuit board,  
and further, the delay time can be continuously adjusted. The delay line can also be  
formed in a multilayer structure rather than on the above dielectric substrate.

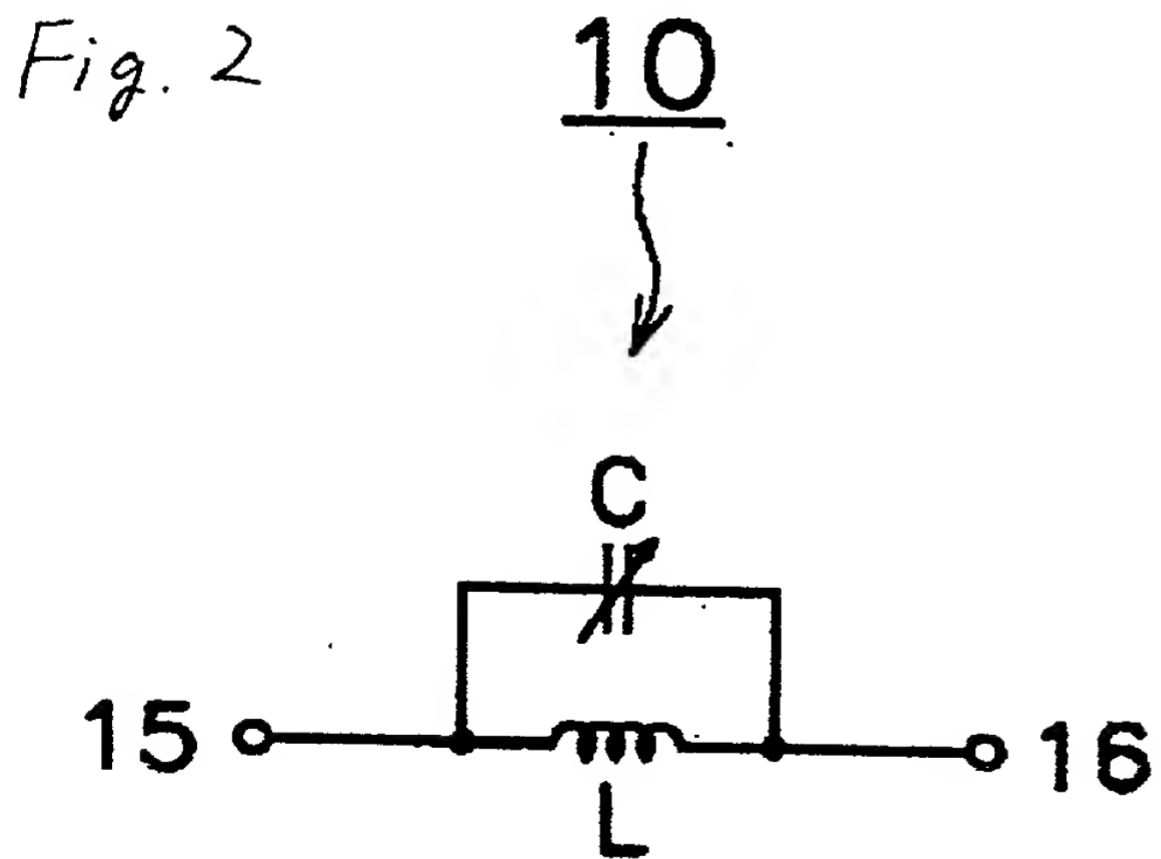
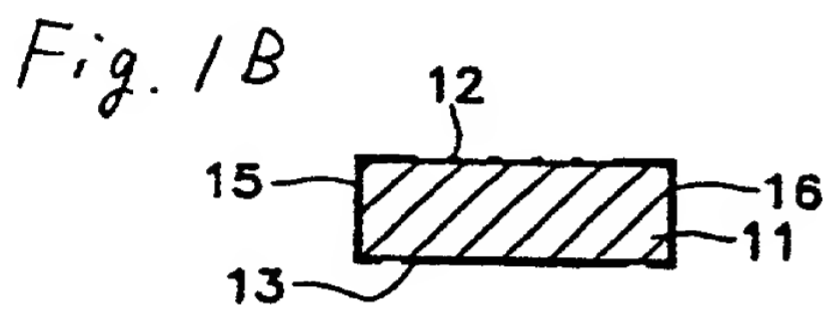
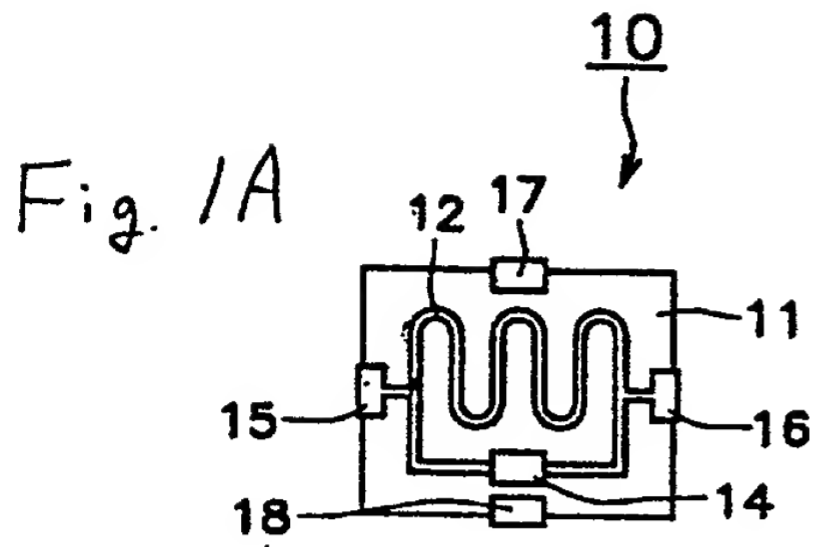


Fig. 3

Pass Characteristics (dB)

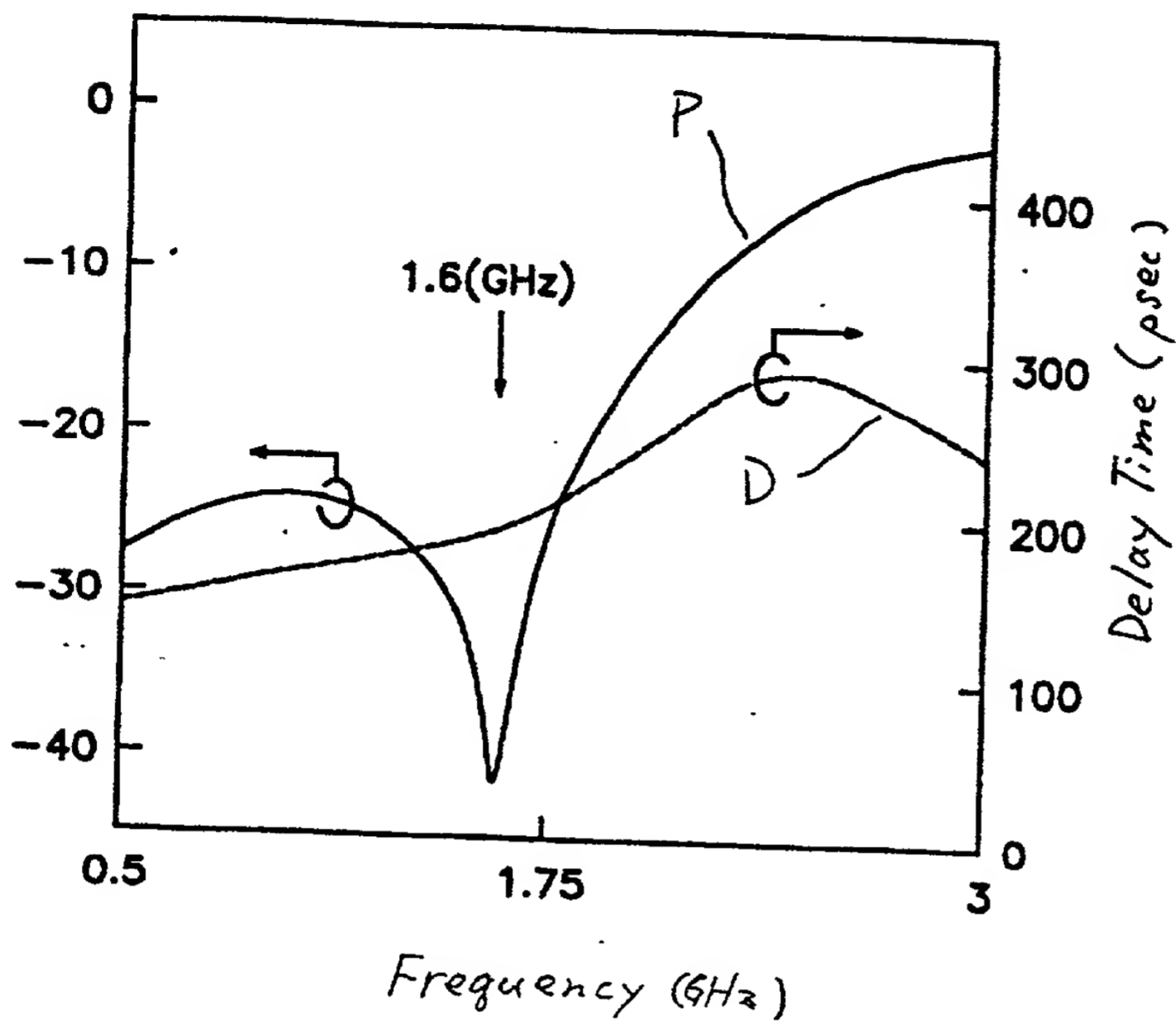
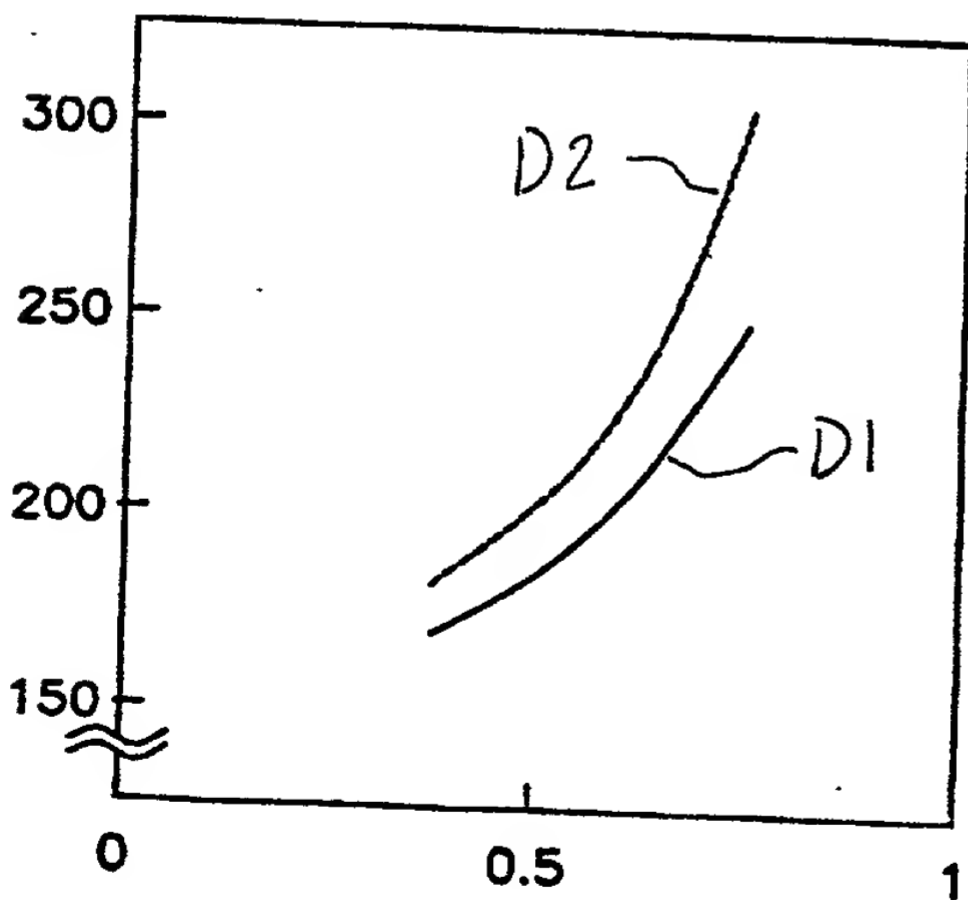


Fig. 4

Delay Time (psec)



Capacitance of Capacitor (pF)

Fig. 5

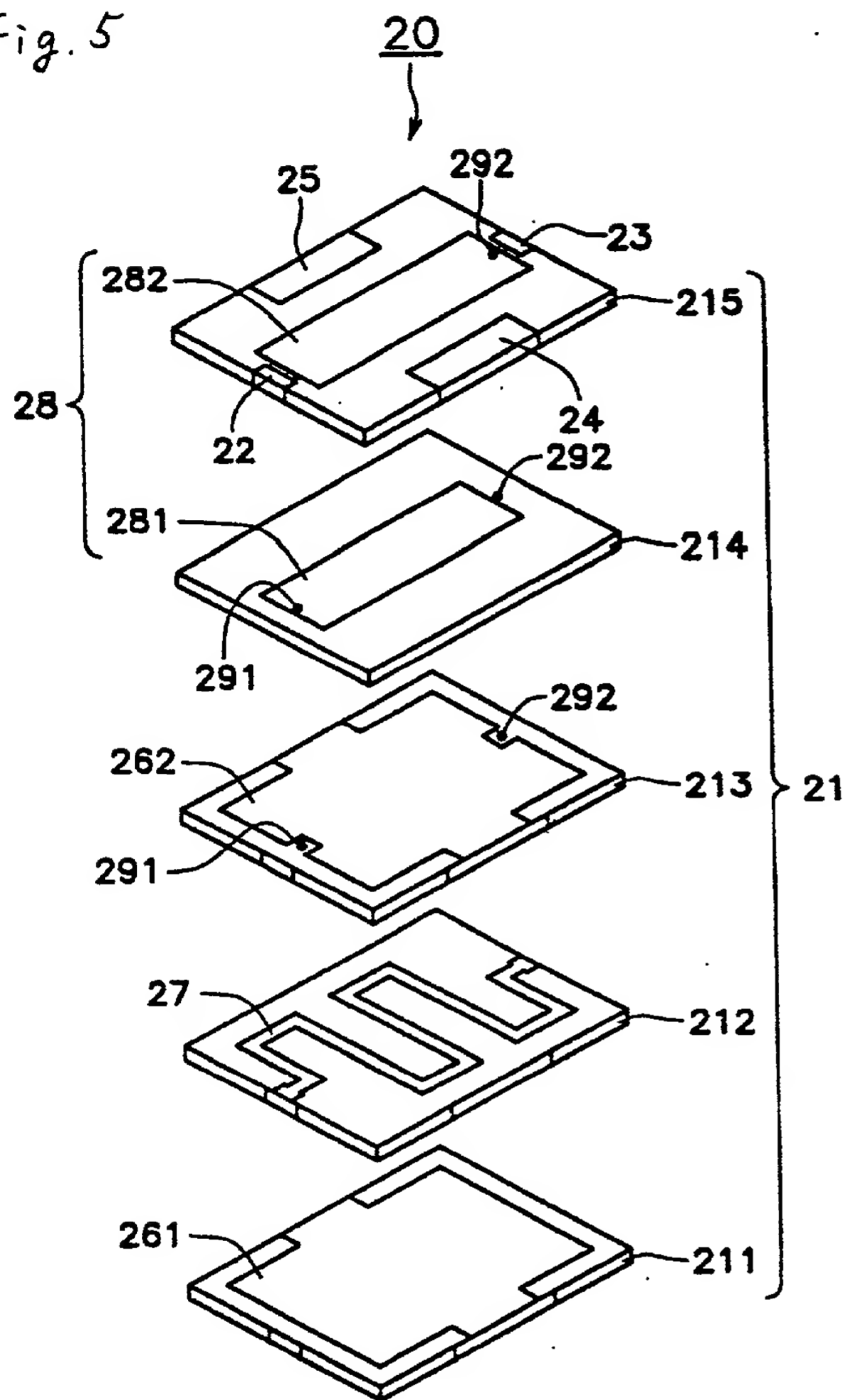


Fig. 6

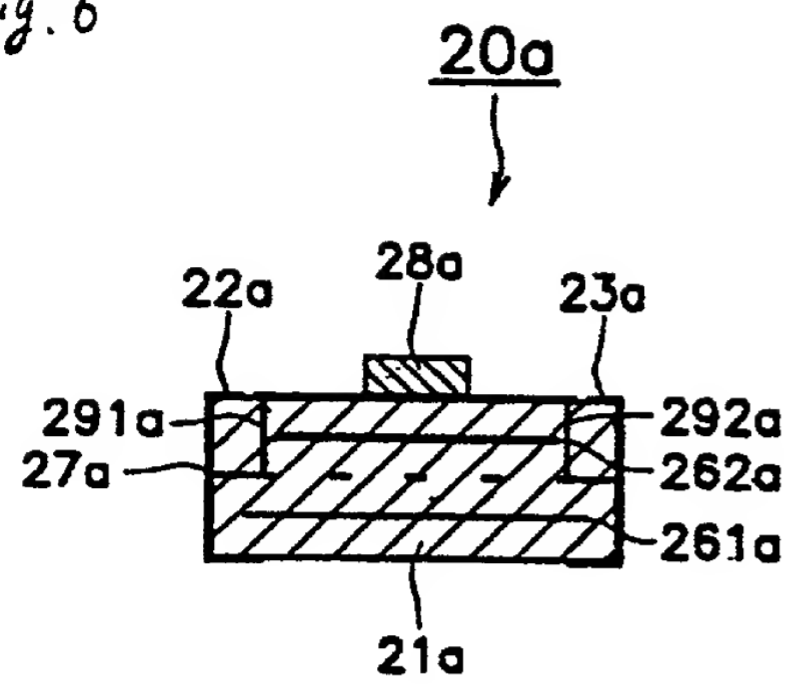


Fig. 7

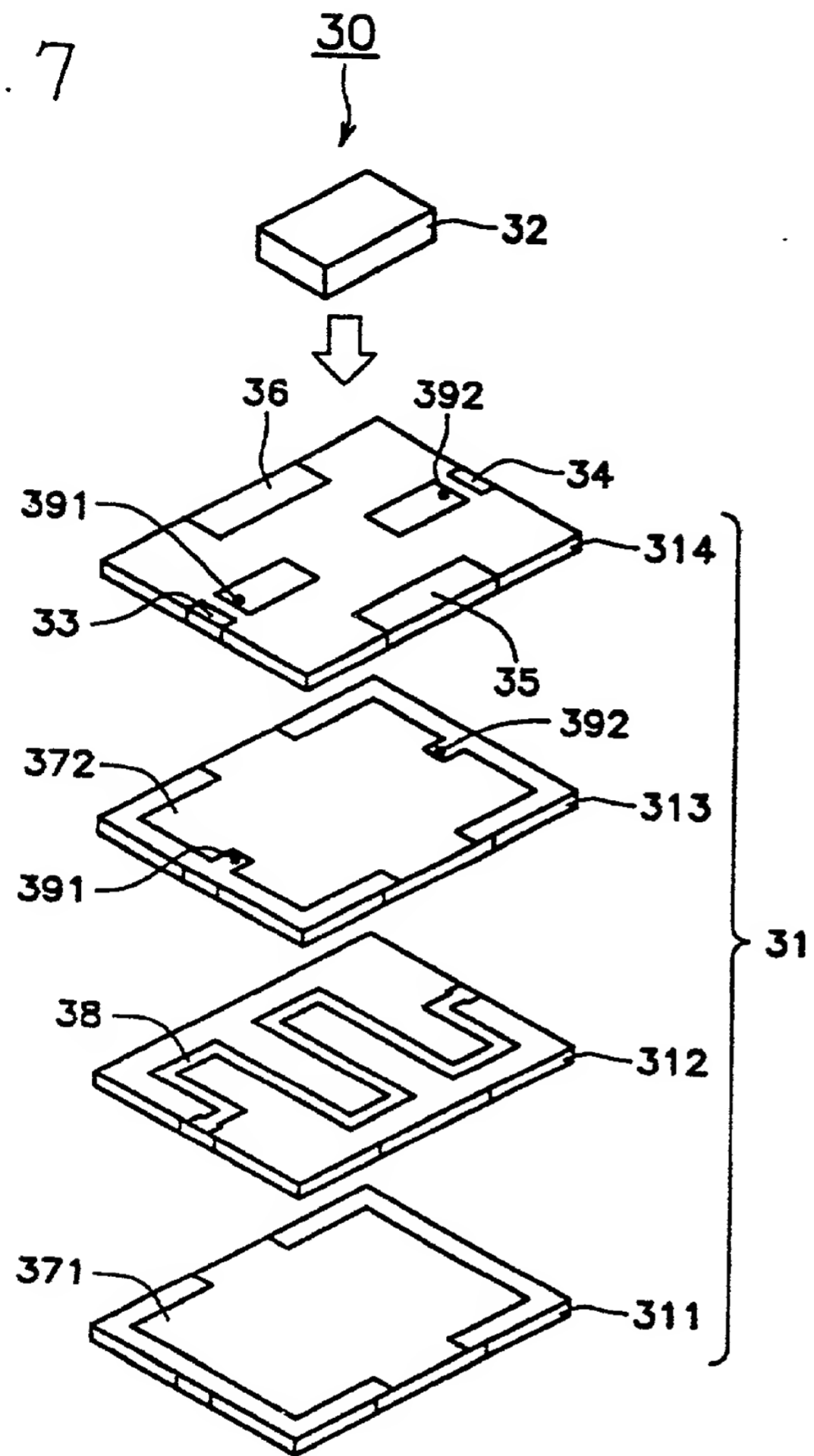


Fig. 8

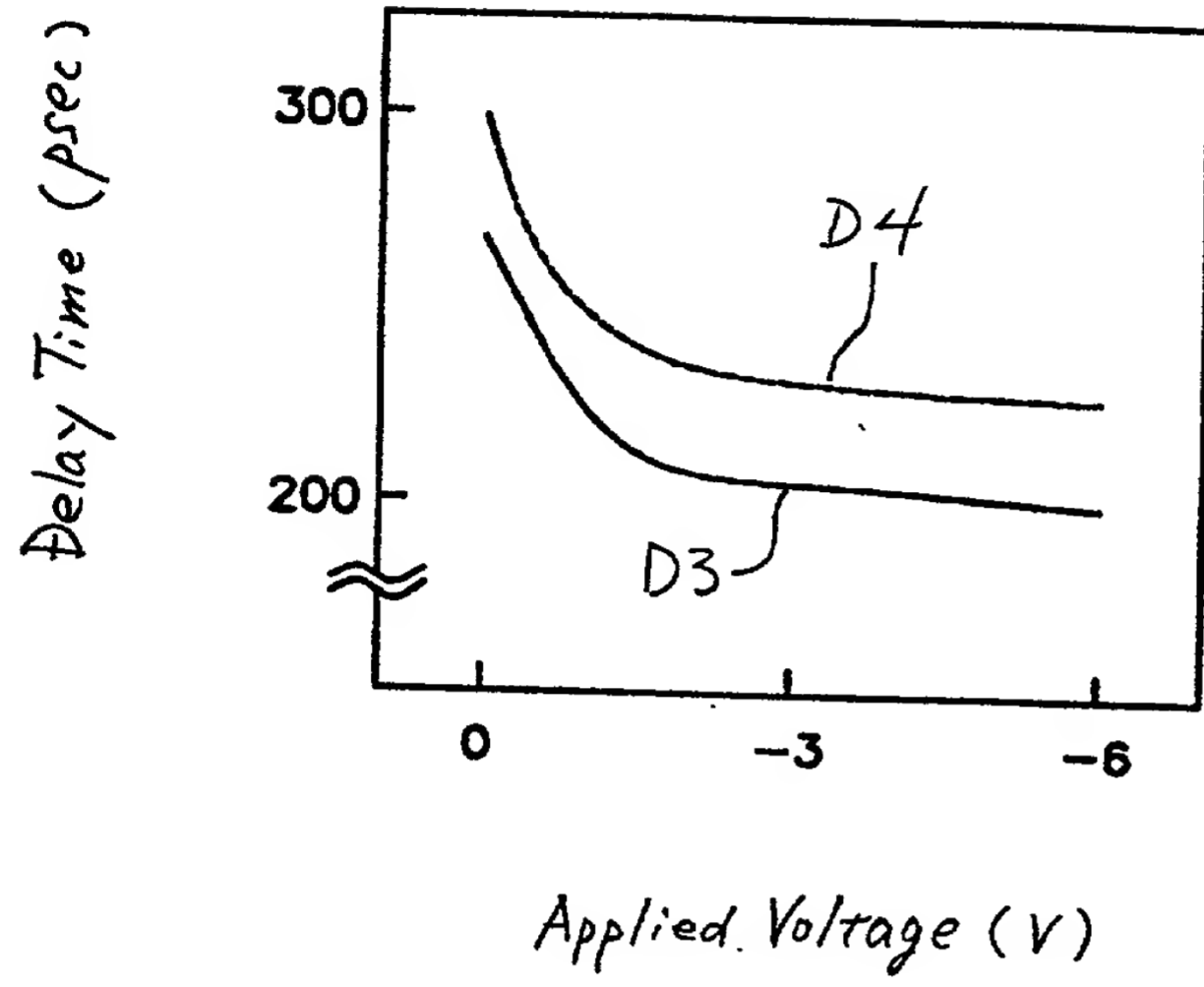
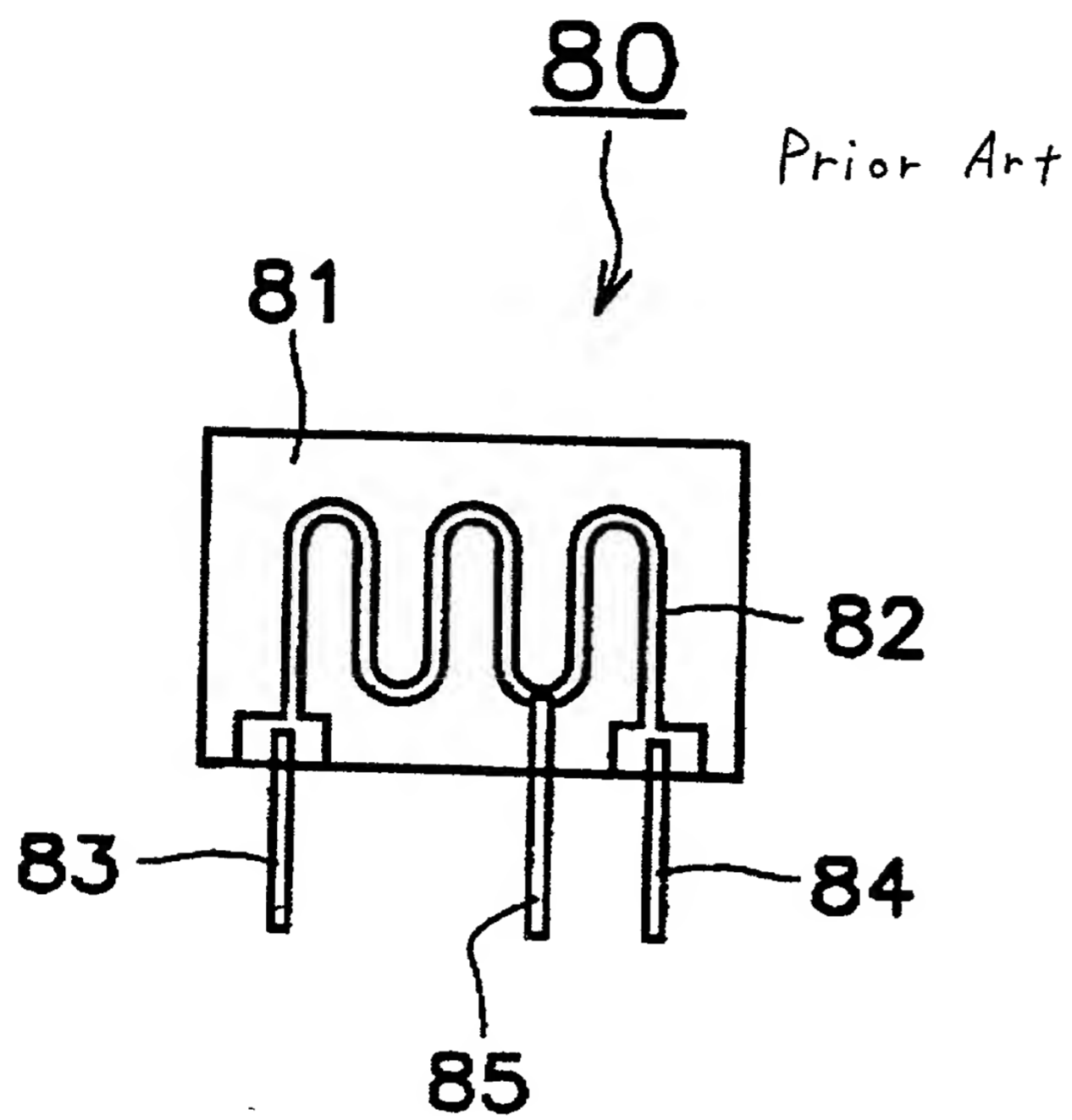


Fig. 9



UNITED STATES OF AMERICA COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION			OFGS FILE NO. P/1071-993																																																							
<p>As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:</p> <p><b>DELAY LINE</b></p>																																																										
<p>the specification of which is attached hereto, unless the following box is checked:</p> <p><input type="checkbox"/> was filed on _____ as United States patent Application Number or PCT International patent application number _____ and was amended on _____ (if any).</p> <p>I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.</p> <p>I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.</p> <p>I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:</p> <p>Prior Foreign or Provisional Application(s)</p> <table border="1" style="width: 100%; border-collapse: collapse;"><thead><tr><th style="width: 25%;">COUNTRY</th><th style="width: 25%;">APPLICATION NUMBER</th><th style="width: 25%;">DATE OF FILING (day, month, year)</th><th style="width: 25%;">PRIORITY CLAIMED UNDER 35 U.S.C. 119</th></tr></thead><tbody><tr><td>Japan</td><td>11-154044</td><td>1 June 1999</td><td>YES <input checked="" type="checkbox"/> NO <input type="checkbox"/></td></tr><tr><td> </td><td> </td><td> </td><td>YES <input type="checkbox"/> NO <input type="checkbox"/></td></tr><tr><td> </td><td> </td><td> </td><td>YES <input type="checkbox"/> NO <input type="checkbox"/></td></tr></tbody></table> <p>I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.</p> <table border="1" style="width: 100%; border-collapse: collapse;"><thead><tr><th style="width: 33%;">UNITED STATES APPLICATION NUMBER</th><th style="width: 33%;">DATE OF FILING (day, month, year)</th><th style="width: 34%;">STATUS (patented, pending, abandoned)</th></tr></thead><tbody><tr><td> </td><td> </td><td> </td></tr><tr><td> </td><td> </td><td> </td></tr><tr><td> </td><td> </td><td> </td></tr></tbody></table> <p>I hereby appoint customer no. 2352 OSTROLENK, FABER, GERB &amp; SOFFEN, LLP, and the members of the firm, Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A. McIlman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,400; Steven I. Weisburd - Reg. No. 27,409; Max Moskowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063; James A. Finder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944; Louis C. Dujmich - Reg. No. 30,625 and Douglas A. Miro - Reg. No. 31,643, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent &amp; Trademark Office connected therewith and to receive all correspondence.</p> <p>SEND CORRESPONDENCE TO: <b>OSTROLENK, FABER, GERB &amp; SOFFEN, LLP</b> DIRECT TELEPHONE CALLS TO: 1180 AVENUE OF THE AMERICAS (212) 382-0700 NEW YORK, NEW YORK 10036-8403 CUSTOMER NO. 2352</p> <p>I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.</p> <table border="1" style="width: 100%; border-collapse: collapse;"><tr><td style="width: 40%;">FULL NAME OF SOLE OR FIRST INVENTOR Teruhisa TSURU</td><td style="width: 30%;">INVENTOR'S SIGNATURE <i>Teruhisa Tsuru</i></td><td style="width: 30%;">DATE May 8, 2000</td></tr><tr><td colspan="2">RESIDENCE (City and either State or Foreign Country) Kameoka-shi, Kyoto-fu, Japan</td><td>COUNTRY OF CITIZENSHIP Japan</td></tr><tr><td colspan="3">POST OFFICE ADDRESS c/o Murata Manufacturing Co., Ltd., Dept. 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